Adaptive Support Weight Based Stereo Matching Accelerator

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I. INTRODUCTION

Stereo matching is a core technology applied to various 3D vision processing systems such as intelligent robot vision systems, autonomous vehicle systems, 3D broadcast systems and mobile devices. Most recent researches have been focused on the development of algorithm-centric vision systems based on the CPU or the GPU. There are some researches and developments for the implementation of hardware accelerators of stereo matching, but most of them are only about production of depth maps using FPGA devices which have constraints in cost and performance. On the other hand, there are few researches and developments for ASIC implementation of stereo matching. So, for low-power and small-area implementation, we developed a stereo matching accelerator as an ASIC.

II. DESCRIPTION

A. *Description System Architecture*

Fig. 1 shows the block diagram of the proposed stereo matching accelerator based on adaptive support weight, which consists of three blocks. The Pre-Processing block produces noise-removed images for the generation of reliable 3D depth maps. The Depth Extraction block produces 3D depth maps using Census transform algorithm [1] and adaptive support weight algorithm [2]. Finally, the 3D depth maps are de-noised by the Post-Processing block. The generated 3D depth maps are used for the extraction of distance.

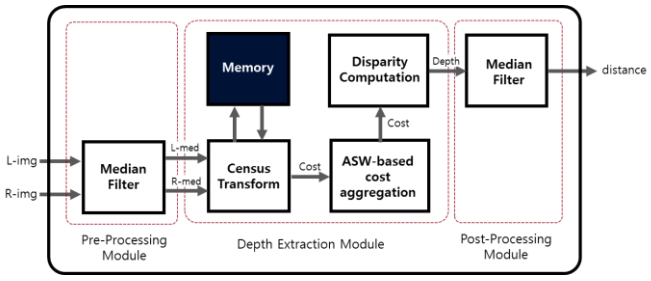

Fig. 1. Block diagram of the stereo matching accelerator.

B. *Design and Implemention*

The proposed stereo matching accelerator was described and designed with Verilog HDL and verified by FPGA implementation. The test images of the Middlebury image sets [3] were used for this FPGA verification.

III. CHIP IMPLEMENTAION AND RESULTS

After the FPGA verification, the stereo matching accelerator was implemented in an ASIC through the IDEC MPW program with Samsung 65 nm technology. Table 1 shows the detailed specifications of the developed ASIC, and Fig. 2 shows its layout and ASIC picture.

Specifications	
Gate count	6860000
Frequncy	74.25 MHz
SRAM	64 SRAMSs of 752 × 8
die size	4 mm × 4 mm

Table 1. Chip specifications.

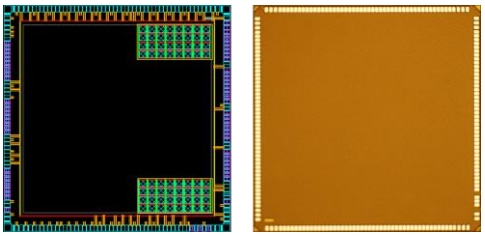

Fig. 2. Layout and ASIC picture of the stereo matching accelerator.

REFERENCE

[1] S. Jin, J. Cho, X. D. Pham, K. M. Lee, S. –K. Park, M. Kim, and J. W. Jeon, "FPGA Design and Implementation of a Real-Time Stereo Vision System," IEEE Transactions on Circuits and Systems for Video Technology, vol. 20, no. 1, pp.15-26, Jan. 2010.

[2] N. Y.-C. Chang, T.-H. Tsai, B.-H. Hsu, and Y.-C. Chen, "Algorithm and architecture of disparity estimation with mini-census adaptive support weight, IEEE Transactions on Circuits and Systems for Video Technology, vol. 20, no. 6, pp. 732-805, Jun. 2010.

[3] Middlebury Stereo Vision Page, http://vision.middlebury.edu/stereo/.

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